DESIGN TECHNIQUES FOR GaAs MESFET SWITCHES

G. J. Gardiner, M. W. Geen, D. C. Smith

Plessey Three Five Group Ltd, Towcester, Northants, UK

ABSTRACT

A three port bias dependent model for a switch FET is presented. The importance of a three port model is highlighted. Large signal behaviour of a MESFET switch in its ON and OFF states is discussed. The effect of gate bias resistor and bias potential is illustrated. Simple equations and techniques are presented which enable estimates of power performance of complex switches to be made prior to detailed non-linear analysis.

INTRODUCTION

During recent years the GaAs MESFET has gained increasing favour as a switching element in control circuits such as phase shifters, routing switches and attenuators (1,2,3,4). This is particularly evident in multifunction monolithic integrated circuits where the rival PIN diode is generally incompatible with established MMIC foundry technology. The advantages of MESFET switches: low power consumption, fast switching speed and broadband performance are well known (5), but to take full advantage of the devices capability and obtain optimum circuit performance, it is essential to understand their behaviour at large signal levels and under a variety of bias conditions (6). This paper will present a bias dependent 3 port model for the MESFET switch based on extensive measurements of ion implanted devices manufactured using established MMIC processes. The effect of a gate isolating resistor (essential in most practical applications) on the large signal performance will be described. Expressions, which allow 1dB compression points to be estimated are given and verified by comparison with mesurements of two different geometry switch FETs. Finally, the rarely reported subject of isolation performance at large signal levels is discussed.

SWITCH FET CHARACTERISATION

MESFETs used in attenuators or switches invariably have a high value r.f blocking resistor connected in their gate circuit. The resistor is essential to good circuit performance. This being the case, it remains necessary to characterise the FET as an isolated component, ideally in its grounded gate configuration. A three port equivalent circuit model of the switch FET is shown in Fig. 1. The presence of the gate resistor, Rgb, as part of the basic characterisation element renders Cgc and Cds indistinguishable. It is not possible to strip the effect of the resistor after a 2 to 3 port S-parameter transformation of the measured data, because the reactance of the unknown, parasitic shunt capacitances (Cp) appear in parallel with Rgb and have similar impedance. Measurement of the bare FET in common source connection is not ideal because the grounding source via eliminates the effect of Cp.

In our measurements the gate of the switch FET was directly grounded by means of a via hole in the GaAs substrate. Devices were measured as series components. Gate to channel bias Vgc, derived from a single voltage source, was applied simultaneously to source and drain through bias tees. Applying bias solely to source or drain, leaving the unused bias-T open circuit, resulted in a voltage between source and drain at bias points near or beyond Vp. This was manifested as degraded isolation performance and severe asymmetry in S11 and S22. The power level used in the measurement system is critical. Non-linear behaviour has been observed at power levels as low as 0dBm in a 300µm wide FET biased near pinch-off.

The quality of characterisation data, after stripping test fixture parasitics, can quickly be assessed. Primarily the data should be smooth. The FET under switch bias conditions is passive, and hence reciprocal, therefore the condition S12 = S21 should be satisfied. Furthermore, the common gate FET has considerable geometric symmetry which is reflected in the observation that S11 ≈ S22. The FETs characterised to obtain the present results satisfied this condition well and the equivalent circuit model was taken to be symmetric.

Characterisation data was recorded at 20 bias points and concentrated on regions where FET characteristics changed rapidly. It was found that the switch FET can be described well at bias conditions between Vgc <+0.6V and Vgc >-Vb (Vb = breakdown voltage) by 3 non-linear elements Rc, Cgc and Rgc (Fig. 1). Rgc is only significant when the gate to channel Schottky becomes forward biased.

TOUCHSTONE™ was used to fit the equivalent circuit to the measured data. Resistance values were chosen to fit low frequency (45MHz - 500MHz) characteristics. When the FET is biased well beyond pinch off ($Rc>>1x10^6$) and at low frequencies XLg is small, only Cds couples source and drain. This enabled Cds to be accurately extracted. Cds is determined by geometry and is influenced by gate recess

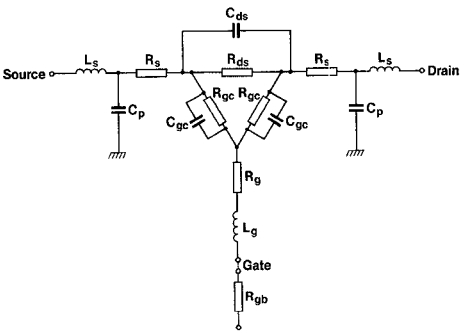

Figure 1 Equivalent circuit of a MESFET switch.

length. Cgc and Lg cause roll-off in S21 at high frequencies and bias voltages less than Vp. Lg is bias independent which enables Cgc to be extracted.

Fig. 2 shows the variation of Cgc and Rc with bias for a 300 μm switch FET. The exceptionally abrupt increase in Rc near Vp reflects a sharp reduction in doping concentration between the channel and the substrate, a valuable feature achieved using a novel implantation scheme. Note also the wide range of channel resistance (10:1) making the device a useful voltage controlled resistor. A plot of 1/Rds vs Vgc is virtually linear to Vgc = 3V.

Fig. 3 shows agreement achieved between modelled and measured S-parameters at an intermediate bias point. Fig. 4 shows agreement in modelled and measured insertion loss at several bias points.

EFFECT OF R.F. BLOCKING RESISTOR

i) Small Signal Performance

The value of a 3-port switch FET model is now illustrated. The resistor Rgb has a critical effect upon small signal performance, large signal performance and switching speed. It is assumed in the following discussion that the FET is connected in series with source and load. (It is a straightforward matter to infer the behaviour of a FET in a shunt configuration). The size of Rgb affects small signal insertion loss, (Fig. 5), and isolation. The 3 port model enables the effect of Rgb to be assessed. Complex designs may involve many FETs controlled from a common bias point and the 3 port model is necessary to evaluate device interaction. Switching speed is proportional to the product, Cgc Rgb, and a trade-off exists between switching speed, insertion loss and isolation.

ii) Large Signal Performance 'ON' State

Fig. 6 shows the variation in 1dB insertion loss compression as a function of frequency. Two breakpoints exist in the large signal insertion loss characteristic fL and fH. The frequency fL is estimated by assuming it occurs when an appreciable rf signal is dropped across Rgb

$$fL = \frac{1}{2\pi Rgb\ (2Cgc)}$$

Experimentally, it is found that $P_{(-1}{}^{dB}{}_{)}$ of a single series connected FET switch increases at approximately 2.5dB per octave above fL until the high frequency compression mechanism dominates.

When Vgc = 0V the characteristic can be interpreted as follows (see Fig. 7): In the low frequency region, XCgc >>Rgb, negligible current flows in Rgb. A positive voltage cycle at A sets up voltages VL and VF. VL reverse biases the gate Schottky, current saturation occurs, limiting power to the load. With a negative cycle at A, the gate Schottky is forward biased: current saturation occurs at a much higher level, either when the device is thermally overloaded or by charge carrier velocity saturation beneath the gate when the electric field significantly exceeds 0.25V per micron. A rectified current flows in Rgb. In the low frequency region compression occurs by asymmetric clipping of the r.f. waveform, (Fig. 8).

Power performance at low frequencies is highly bias dependent as can be deduced. Table 1 shows the variation in output power at 1dB gain compression as a function of gate control voltage for a 300μm wide FET with Rgb = 8000 at 10MHz. This behaviour has implications on the design of circuits such as voltage controlled attenuators.

Vgc/V	Insertion loss	Output power at $P_{(-1)}/dBm$
10	0.92	27.4
1	0.92	20.8
0.5	1.00	19.8
0	1.00	18.4
-0.5	1.00	18.1
-1.0	1.28	15.6
-2.0	1.90	11.0
-2.5	2.40	6.7

In the high frequency region, XCgc <<Rgb the potential of the gate is approximately VL + VF/2 (Vgc = 0). While VF is small, one end of the gate is reverse biased by VF/2, the other forward bias by VF/2, as Cgc's at 'either end of the gate' are equal and form a potential divider. The negative feedback effect of RL is eliminated. As the signal applied to the FET is increased, the potential at the gate will fall towards VL with a positive signal at A, due to the voltage dependent nature of the 'two' gate channel capacitances. When VF = Vth, the threshold voltage of the FET, current saturation will occur, the saturated current will be greater than Idss because the gate to source junction is effectively forward bias. Compression is by symmetric clipping of the r.f. waveform, (Fig. 9).

iii) Estimating High and Low Frequency 1dB Compression Point for Switches in the ON State

At low frequencies the current in RL can be approximated by

$$iL = Io \sin \omega t \text{ when } Io\sin \omega t < Isat$$
$$\text{and } iL = Isat \text{ when } Io\sin \omega t > Isat$$

The power dissipated in a 50 load can be compared with the power which would be dissipated had a sinusoidal current been present. Adjusting Io until

$$10\left[\text{Log}\ (50Io^2/2)/\left(\frac{50}{2}\right)\int_0^{2\pi} i_L{}^2(t)dt\right] = 1$$

$$P_{(-1)}/dBm \simeq 20 \log\ (Isat/mA) - 12.21$$

Isat is taken from the bare FET using a plot of Vg/Ids versus Ids (Vds greater than threshold). Isat occurs at the point where Vgs/Ids = RL on this plot.

For symmetric clipping

$$P_{(-1)}/dBm \simeq 20 \log\ (Isat/mA) - 13.89$$

$$Isat \simeq Ids\ (Vgc=+0.4V, Vds>Vth)$$

Table 2 shows a comparison between measured and estimated compression points for 300 and 600μm wide switch FETs.

Product (FET)	P35-4205 (300μm)	P35-4210 (600μm)	Unit
PL measured	17 to 19	19 to 21	dBm
PL calculated	18.3	22.0	dBm
fL measured	30	-	MHz
fL calculated	45	-	MHz
PH measured	24 to 26	27 to 32	dBm
PH calculated	25.7	33.0	dBm

LARGE SIGNAL ISOLATION PERFORMANCE

When the FET is in its isolated state Vgc<-Vp, Cgc is small, Rc is large. In Fig. 7 a negative cycle at A acts to reduce the magnitude of Vgc at that end of the channel. When reverse bias drops below Vp, isolation degradation occurs and current flows in the load. A positive cycle at A causes gate channel reverse bias and VF, the voltage across the FET, to increase. Two effects occur, gate to channel breakdown at very large signals, a small but rapidly increasing leakage current in the channel and at much lower signal levels. Variation in isolation with control voltage and power of a 300μm FET is shown in Fig. 10.
The optimum control voltage depends on several inter-related factors, particularly Vp. Ideally Vp should be as small as possible. Vp is related to implantation depth and doping concentration as is insertion loss in the low loss state. Breakdown voltage is inversely proportional to doping concentration. For a given breakdown voltage and minimum insertion loss Vp can be limited by reducing the extent of the 'tail' on the implantation profile. The tail has a significant effect on Vp and leakage current and has been limited substantially by Plessey Three Five using a novel implantation scheme. In practical applications the magnitude of the control voltage will be chosen to be as small as possible to ease driver specification and compatibility with the required power handling capacity.

CONCLUSIONS

A large signal, bias dependent, 3-port analysis of switch FET modelling has been presented. The models provide circuit designs with the ability to estimate large signal power handling characteristics of MMIC switch designs, without immediate recourse to complex non-linear CAD.

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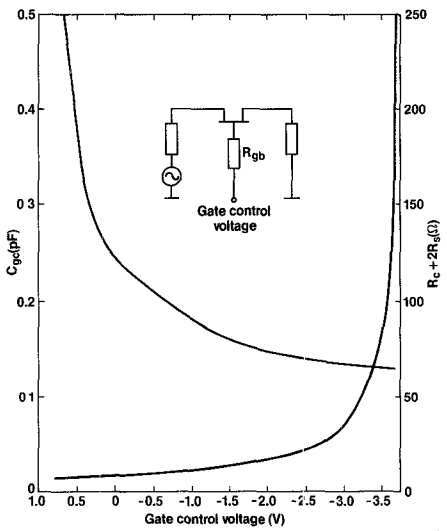

Figure 2 Variation of gate to channel capacitance C_{gc}, and total FET series resistance $R_c + 2R_s$ as a function of gate to channel voltage.

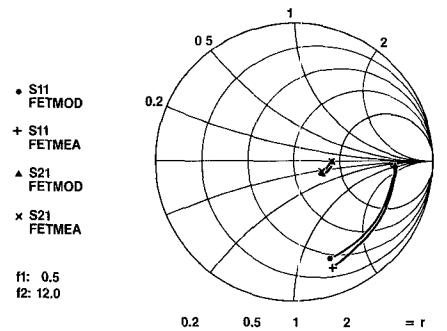

Figure 3 Agreement between modelled and measured s-parameters of a series MESFET switch with channel biased close to pinch-off.

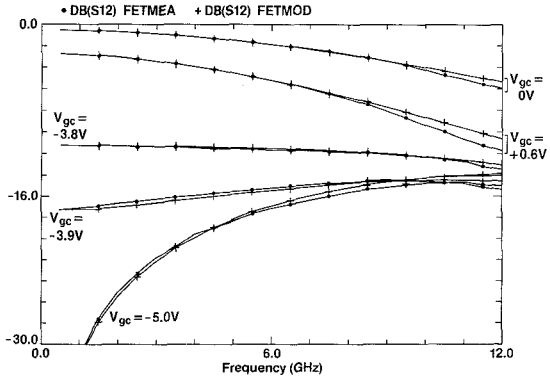

Figure 4 Comparison of modelled and measured insertion loss performance of a common gate switch FET at various gate to channel voltages.

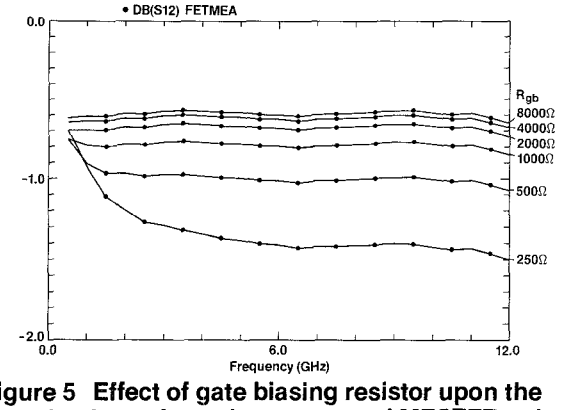

Figure 5 Effect of gate biasing resistor upon the insertion loss of a series connected MESFET switch in its low loss state.

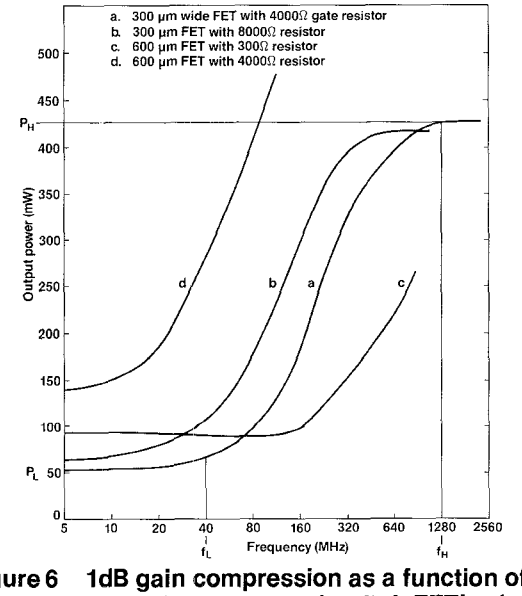

Figure 6 1dB gain compression as a function of frequency for series connected switch FET's shows the effect on performance of the gate blocking resistor.

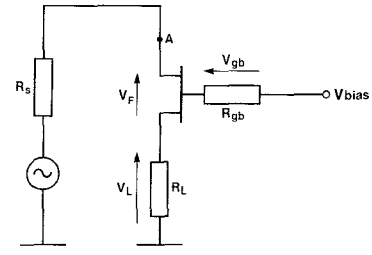

Figure 7 Voltages associated with a series connected FET switch.

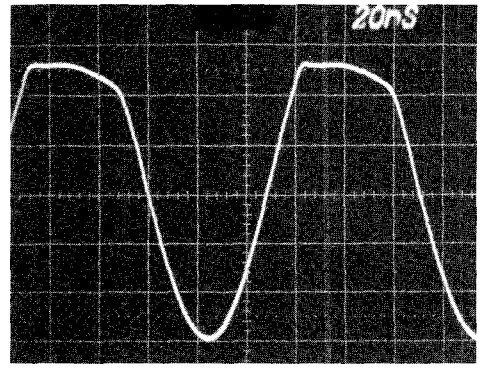

Figure 8 Asymmetric clipping of r.f. wave form in the load of series connected FET switch in the low loss state at "low frequencies".

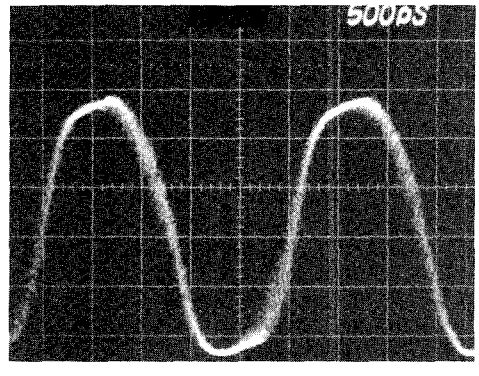

Figure 9 Symmetric clipping of r.f. waveform in the load of a series connected FET switch in the low loss state at "high frequencies".

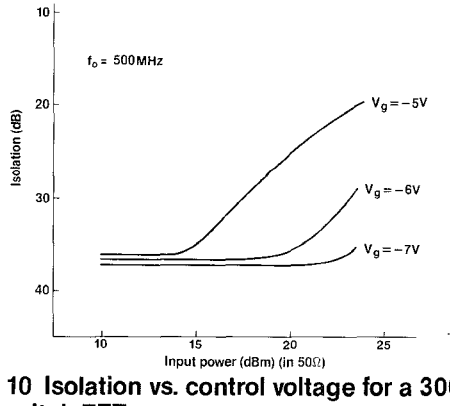

Figure 10 Isolation vs. control voltage for a 300µm series switch FET.